APPLICATION INFORMATION

400 MHz low noise amplifier with the BFG540W/X

Philips
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ABSTRACT

- Description of the product

  The BFG540W/X is one of the Philips silicon planar epitaxial wideband transistors of the BFG500 series.
- Application area

  Low voltage analog and digital UHF-applications in the GHz range.
- Presented application

  A low noise amplifier for CDMA mode of operation for 400 MHz with a low power consumption.
- Main results

  At a frequency of 400 MHz, a supply voltage of 3.0 V and a current consumption of approximately 7.5 mA, the amplifier has an insertion power gain of approximately 15.5 dB, a noise figure of approximately 1.0 dB and a third order intercept point of approximately 2 dBm (measured at input).

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INTRODUCTION

With the Philips silicon wideband transistors BFG540W/X, it is possible to design Low Noise Amplifiers (LNAs) for UHF applications with a low current and a low supply voltage. These amplifiers are well suited for the new generation low voltage high frequency wireless applications. This application note gives an example of an LNA for 400 MHz Code Division Multiple Access (CDMA) mode of operation (Chinese market).

CIRCUIT DESCRIPTION

The following initial conditions apply for the amplifier design:

- V_{supply} = 3.0 V
- V_{CE} = 2 V
- I_C < 10 mA
- f = 400 MHz.

The circuit is designed to show the following performance:

- $|s_{21}|^2 \approx 15$ dB
- $VSWR_{IN} < 2$
- $VSWR_{OUT} < 2$
- NF < 1.5 dB
- $IP3_i > 0$ dBm.

The input and output matching is realised with an LC-combination. Also extra emitter inductance (micro stripline) is used on both emitter leads to improve the matching and the noise figure.

CIRCUIT DIAGRAM

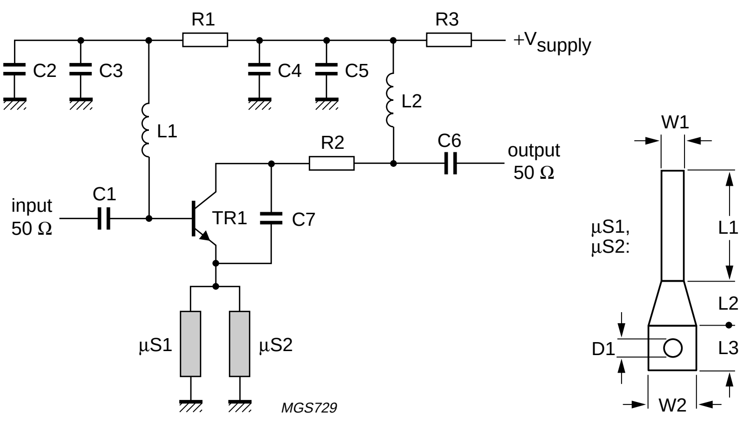

Fig.1 Circuit diagram.

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COMPONENT LIST

Table 1 Component list for the 400 MHz LNA

COMPONENT	VALUE	UNIT	SIZE, MANUFACTURER	PURPOSE, COMMENT
TR1	BFG540W/X		SOT343N Philips	active element
R1	22	kΩ	0603 Philips	collector to base bias
R2	22	Ω	0603 Philips	s_{22} and stability improvement; reducing gain
R3	100	Ω	0603 Philips	collector bias, levelling h_{FE} spread
C1	150	pF	0603 NP0 Philips	input to base match
C2	150	pF	0603 NP0 Philips	400 MHZ short (L1 to ground)
C3	22	nF	0603 X7R Philips	LF short; IP3 improvement
C4	22	nF	0603 X7R Philips	LF short; IP3 improvement
C5	150	pF	0603 NP0 Philips	400 MHZ short (L2 to ground)
C6	8.2	pF	0603 NP0 Philips	collector to output match
C7	4.7	pF	0603 NP0 Philips	collector to emitter output match; stability improvement
L1	22	nH	0805CS Coilcraft	input match; base bias
L2	22	nH	0805CS Coilcraft	output match; collector bias
µS1	see Table 2			emitter induction: micro stripline and via-hole
µS2	see Table 2			emitter induction: micro stripline and via-hole
PCB	FR4			ε_r = 4.6; d = 0.5 mm

Table 2 Dimensions of the micro striplines µS1 and µS2 (see Fig.1)

DIMENSION	VALUE	UNIT	DESCRIPTION
L1	2.5	mm	length micro stripline; $Z_o \approx 48\ \Omega$
L2	1.0	mm	length interconnect micro stripline and via-hole area
L3	1.0	mm	length via-hole area
W1	0.5	mm	width micro stripline
W2	1.0	mm	width via-hole area
D1	0.4	mm	diameter of via-hole

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BOARD LAYOUT

The layout has been designed with the Hewlett Packard Microwave Design System (HP-MDS).

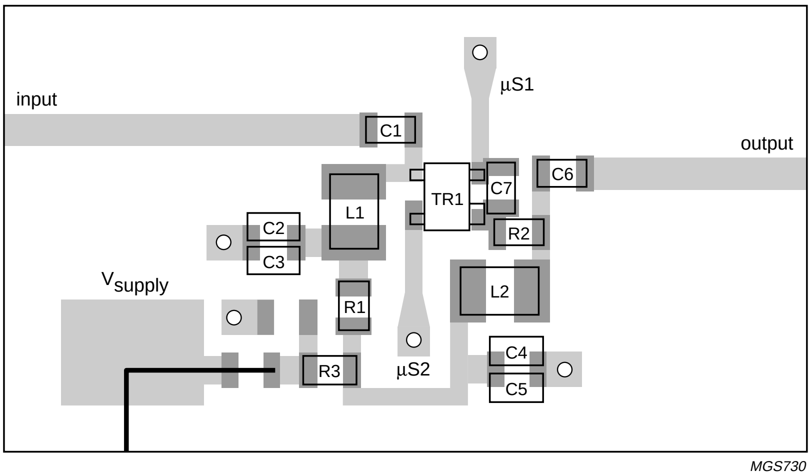

Fig.2 PCB layout.

MEASUREMENTS

Measurements have been done on a simulation model (with realistic RF models of all parts used) as well as on an actual printed-circuit board. The measurements have been done under the following conditions (unless otherwise specified):

- V_{supply} = 3.0 V
- I_{supply} = 8 mA
- f = 400 MHz.

Table 3 Measuring results of the 400 MHz LNA

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$\lvert s_{21}\rvert^2$	insertion power gain	note 1		
		Spice simulation model	15.5	dB
		actual printed-circuit board	15.6	dB
$\lvert s_{12}\rvert^2$	reverse insertion power attenuation	note 1		
		Spice simulation model	–26.2	dB
		actual printed-circuit board	–28	dB
$VSWR_{IN}$	input voltage standing wave ratio	note 1		
		Spice simulation model	1.7	
		actual printed-circuit board	1.8	
$VSWR_{OUT}$	output voltage standing wave ratio	note 1		
		Spice simulation model	1.6	
		actual printed-circuit board	2.0	
NF	noise figure	note 2		
		Spice simulation model	1.3	dB
		actual printed-circuit board	1.0	dB
$IP3_i$	third order intercept point	Δf = 1 MHz; note 3		
		Spice simulation model	6.7	dBm
		actual printed-circuit board	2	dBm

Notes

1. The circuit is stable for all frequencies.
2. The noise figure performance of the actual printed-circuit board is about 0.3 dB lower than the performance of the simulation model. The difference is caused by the fact that the Spice model of the BFG540W/X is not optimized for noise.
3. The $IP3_i$ performance of the actual printed-circuit board is about 4 dBm lower than the performance of the simulation model. The difference is caused by the fact that the Spice model of the BFG540W/X is not optimized for $IP3_i$.

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